SMD Voltage Controlled Crystal Oscillator

Ultra Low Noise VCXO in 5.0 x 3.2 mm Surface Mount Package.

Product description

The SMK5032VCDS is a very high performance VCXO delivering ultra low close-in phase noise for RF/Analog applications and ultra low RMS phase jitter optimised for high speed serial data and digital applications.

Applications

Communications
Base stations
DSL/ADSL
SONET/SDH
WiMAX/W-LAN
Ethernet Wi-Fi

Features

Excellent close-in phase noise performance
Ultra Low Jitter 0.05 to 0.3 ps integrated 12 kHz to 20 MHz
LVCMOS, LVPECL, or LVDS options
Wide frequency range

Specification for electrical appliances

Parameter	3 .3V		Unit
	MIN	MAX	
Supply Voltage(VDD) 5%	3.135	3.465	V
Frequency Range	1	800	MHz
Frequency Stability	±30 ---	±50	ppm
Supply Current /For LVDS	30	80	mA
Absolute Pull Range	±50		ppm
Total Pull Range: Frequency shift from minimum to maximum control voltage	100	250	ppm
Control Voltage: Nominal 1.65V	0	3.3	V
Linearity Control voltage 0.3 to 3V		10	%
Differential Output:Voltage Swing		350	mV
RMS Phase Jitter : Typical integrated 12kHz to 20MHz	0.05	0.3	ps
Rise Time / Fall Time RL = 100 Ω / CL = 10 pF		0.6	ns
Duty Cycle	45	55	%
SSB PHASE NOISE:25°C	77.76	122.88	MHz
10Hz	-73	-67	dBc/Hz
100Hz	-100	-98	
1KHz	-128	-127	
10KHz	-137	-147	
100 kHz	-148	-150	
Storage Temperature Range	-55	125	°C
Storage Temp. Range	-40	85	°C

Specifications subject to change without notice

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5.0*3.2*1.2mm

MANUFACTURING INFORMATION

Line Parameter	Description
Packaging Description	Tape and reel. Standard packing quantity is 4000 per reel
Reflow	Solder reflow process as per attached profile

ENVIRONMENTAL SPECIFICATIONS

Line Parameter:	Description
Mechanical Shock:	MIL-STD-883, Method 2002
Storage Temperature: range	-55 to 125 ˚C
Humidity :	After 48 hours at 85 ˚C ± 2 ˚C 85% relative humidity non-condensing
Thermal Shock:	MIL-STD-883, Method 1011
Vibration:	MIL-STD-883, Method 2007
Gross and Fine Leak:	MIL-STD-883, Method 1014
RoHS Compliant:	Yes

PIN CONNECTIONS

Line Parameter	Description
Pin 1	VCO
Pin 2	E/D* or NC
Pin 3	GND
Pin 4	OUTPUT
Pin 5	COMPLIMENTARY OUTPUT (LVPECL/LVDS only) or NC
Pin 6	VDD
Output Enabled	>70% of VDD on E/D pin, or E/D pin left open (connected to internal pull-up resistor)
Output Disabled	<30% of VDD on E/D pin, or E/D pin to GND
	Total frequency pull depends on resonator frequency used

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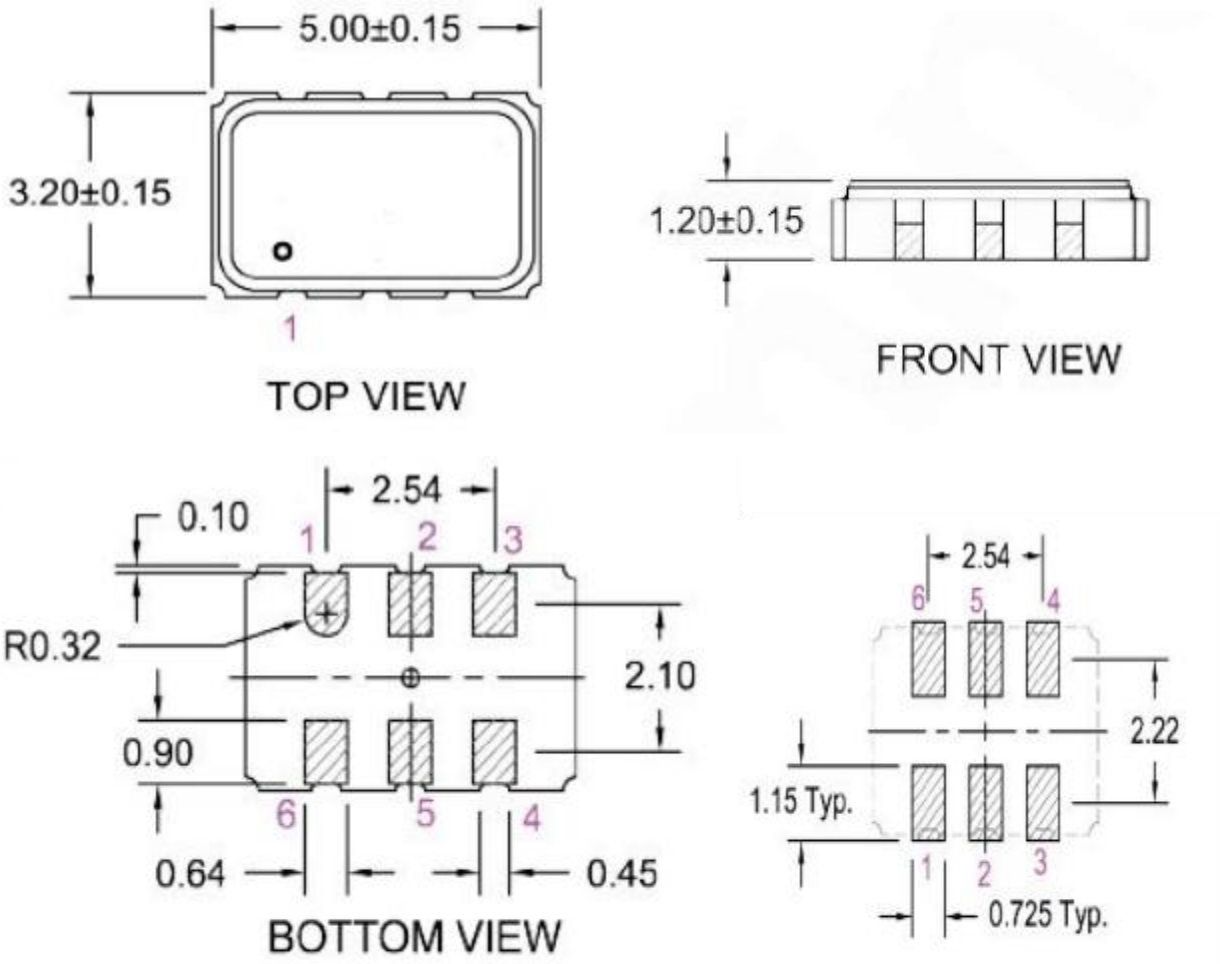
DIMENSION （mm）



NOTE : 1. PIN CONNECTIONS ARE DETAILED IN THE SPECIFICATION.
2. MARKING INFORMATION IS DETAILED IN THE SPECIFICATION.

RECOMMENDED PAD LAYOUT - Top View

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